ISSN 1063-7826, Semiconductors, 2011, Vol. 45, No. 2, pp. 253–259. © Pleiades Publishing, Ltd., 2011.
Original Russian Text © A.E. Belyaev, V.V. Basanets, N.S. Boltovets, A.V. Zorenko, L.M. Kapitanchuk, V.P. Kladko, R.V. Konakova, N.V. Kolesnik, T.V. Korostinskaya, T.V. Kritskaya, Ya.Ya. Kudryk, A.V. Kuchuk, V.V. Milenin, A.B. Ataubaeva, 2011, published in Fizika i Tekhnika Poluprovodnikov, 2011, Vol. 45, No. 2, pp. 256–262.

PHYSICS OF SEMICONDUCTOR DEVICES

Effect of *p–n* Junction Overheating on Degradation of Silicon High-Power Pulsed IMPATT Diodes

A. E. Belyaev[a], V. V. Basanets[b], N. S. Boltovets[b], A. V. Zorenko[b], L. M. Kapitanchuk[c], V. P. Kladko[a], R. V. Konakova[a]^, N. V. Kolesnik[b], T. V. Korostinskaya[b], T. V. Kritskaya[b], Ya. Ya. Kudryk[a], A. V. Kuchuk[a], V. V. Milenin[a], and A. B. Ataubaeva[a]

[a] *V. Lashkaryov Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, pr. Nauki 41, Kyiv 03028, Ukraine*

^e-mail: konakova@isp.kiev.ua

[b] *Orion Research Institute, ul. Eugene Pottier 8a, Kyiv 03057, Ukraine*

[c] *E.O. Paton Electric Welding Institute, National Academy of Sciences of Ukraine, ul. Bozhenko 11, Kyiv 03680, Ukraine*

Submitted July 14, 2010; accepted for publication July 14, 2010

Abstract—The thermal limits of the two-drift impact avalanche and transit-time (IMPATT) diode operating in the pulsed mode in the 8-mm wavelength region with a microwave power as high as 30–35 W have been estimated. It is shown that *p–n* junction overheat at an operating pulse length of 300 ns and a supply current amplitude of 11.3–15 A amounts to 270–430°C relative to an ambient medium. The temperature limit of junction overheating, above which IMPATT diodes rapidly degrade, was determined as 350°C. The presented results of X-ray phase analysis and depth profiles of Au–Pt–Ti–Pd–Si ohmic contact components confirm thermal limits of the IMPATT diode operating in the pulsed mode.

DOI: 10.1134/S1063782611020047

1. INTRODUCTION

Pulsed silicon impact avalanche transit-time (IMPATT) diodes are widely used in various radiolocation, navigation, and control systems and other special-purpose radio-electronic devices [1–6]. An important factor for applications of high-power pulsed IMPATT diodes in microwave circuits is the consideration of features of diode thermal conditions [2, 4, 7]. To avoid diode overheating in the pulsed mode, the input power pulse should be shorter than the thermal relaxation time of the mesa structure mounted on the integral heat sink [2, 4].

In [4, 8], the overheat of high-power silicon IMPATT diodes with a two-drift p^+–p–n–n^+ structure and an active area of 2×10^{-4} cm^2, operating in the 8-mm wavelength region at a supply current density of 20 kA/cm^2 and a pulse duration of 300–400 ns, was estimated as 250–300°C. At the same time, it has long been shown that the temperature (T) dependence of the mean time to failure (D) of the *p–n* junction of the IMPATT diode is given by $\log D = 10 - T/40$ K [9]. This dependence suggests that the IMPATT diode lifetime decreases by an order of magnitude as the *p–n* junction temperature increases by each 40 K.

Since many practical problems require high-power pulsed millimeter-wavelength IMPATT diodes with an output microwave power above 20 W and current densities up to 40 kA/cm^2, determination of their overheating conditions depending on the pulse duration seems urgent. In this case, it is also very important to study physicochemical processes in ohmic contacts and their stability to overheating, since the latter controls in many respects catastrophic failures of IMPATT diodes in devices. Therefore, the objective of this research is to estimate the overheating temperature of the high-power silicon two-drift pulsed millimeter-range IMPATT diode and study the effect of the overheating temperature on interfacial interactions in Au–Pt–Ti–Pd–Si ohmic contacts in which Pt and Ti layers are diffusion barriers.

2. SAMPLES AND METHODS

Samples of two types were studied: test structures and IMPATT diodes fabricated on thin epitaxial structures. The test Au–Pt–Ti–Pd–(p^+)-Si structures were grown by thermal (Pd) and magnetron (Ti–Pt–Au) sputtering of metals onto a thermally cleaned (p^+)-Si (hereafter Si) surface at a substrate temperature of 300°C. In such structures, before and after rapid thermal annealing (RTA) for 60 s at 450°C and thermal annealing (TP) in vacuum at 350(450)°C for 10 min, which simulate IMPATT diode overheating conditions, concentration depth profiles of metallization layer components were measured by Auger electron spectrometry; the phase composition and surface morphology of the Au film were measured by X-ray

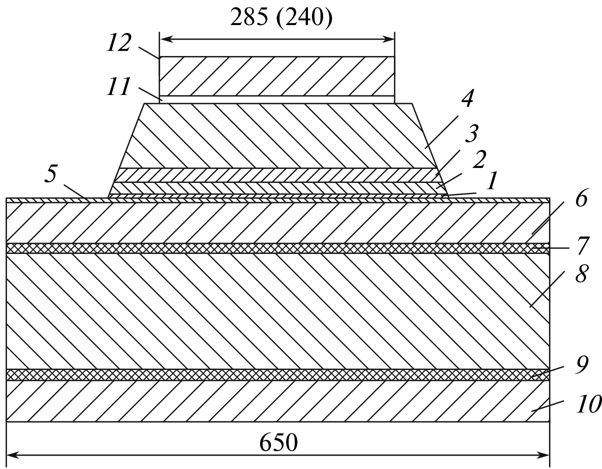


Fig. 1. Structure of the silicon IMPATT diode chip: (*1*) p^+ region; (*2*) and (*3*) drift *p*- and *n*-regions, respectively; (*4*) n^+ substrate; (*5*) Pd–Ti–Pt–Au contact system deposited to the p^+ region; (*6*), (*10*), and (*11*) galvanic gold layers; (*7*) and (*9*) nickel barrier layers; (*8*) copper heat sink; and (*12*) contact system deposited to the p^+ region. Diameters are indicated in micrometers.

diffraction (XRD) and electron microscopy, respectively.

IMPATT diodes of the 8-mm wavelength region and test structures were fabricated based on p–n–n^+ epitaxial structures with the n^+ substrate resistivity of 0.002–0.003 Ω cm [8]. The p^+-Si layer was fabricated by boron diffusion. The boron concentration in the p^+ layer was $\sim 2 \times 10^{20}$ cm^{-3}, the p^+ layer thickness was ~0.3 μm. The thicknesses of epitaxial *p*- and *n*-type layers were 0.95 and 1.15 μm, respectively; the acceptor and donor impurity concentrations in them were identical, 3×10^{16} cm^{-3}. Ohmic contacts to the p^+- and n^+-type silicon layers were grown by depositing Au–Pt–Ti–Pd layers. Diodes were fabricated with integral heat sinks. The diode chip structure is shown in Fig. 1.

The frequency and output power of packaged IMPATT diodes were measured in the pulsed mode at a microwave pulse duration of 300 ns (by the level of 0.5).

The overheating and maximum acceptable duration of the operating current pulse of the high-power silicon pulsed IMPATT diode were estimated using the thermal model [10–12].

3. METHODOLOGICAL ASPECTS OF ESTIMATION OF THERMAL LIMITS OF THE PULSED MODE OF THE IMPATT DIODE

Figure 2 shows the schematic representation of the IMPATT semiconductor mesa structure on a copper heat sink. Region I consists of a p^+ silicon substrate and an epitaxial *n*-layer. Region II includes *p*- and

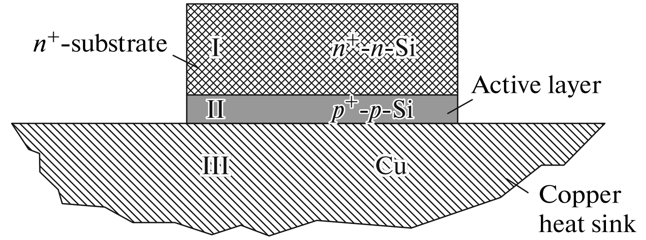


Fig. 2. Schematic representation of the mesa structure of the silicon IMPATT diode on the copper heat sink used in thermal calculations.

p^+-type silicon layers, region III is the copper heat sink. Heat losses in contact ohmic metal layers were disregarded.

It is assumed that the thermal power *P* is released in an infinitely thin layer in the *p*–*n* junction region. At the pulse duration $t_i \le (2–3)\tau_{r1}$, where $\tau_{r1} = l_1^2/4\chi_1$ is the thermal relaxation time of region I, $l_1 = 10$ μm is the thickness of region I, and χ_1 is the thermal diffusivity of region I material (silicon); heat flows propagate in regions I and II according to the temperature gradients in these regions. From region II, the heat flows to heat sink III. In region I, heat is accumulated during the current pulse t_i; in the pause between pulses t_p, heat from region I is transferred to heat sink III. Simultaneously with the above thermal processes, the diode is heated by the average supply power $P_{av} = P_i/Q$ by $\Delta T_{av} = R_{TP}P_{av}$, where R_{TP} is the diode thermal resistance under steady-state conditions, *Q* is the duty ratio, and P_i is the pulsed power. Thus, for the time t_i, the diode active layer temperature increases by

$$\Delta T = \Delta T_i + \Delta T_{av}, \tag{1}$$

where $\Delta T_i = R_iP$ is the time-dependent component of the total diode heating and $P = P_i - P_i/Q = P_i(Q - 1)/Q$ is the ac component of the pulse power. Equation (1) can be written as

$$\Delta T = P_iR_T = P_i\left(R_{Ti}\frac{Q-1}{Q} + \frac{R_{TP}}{Q}\right). \tag{2}$$

It follows from (2) that the transient thermal impedance of the IMPATT is given by

$$R_T = R_{Ti}\frac{Q-1}{Q} + \frac{R_{TP}}{Q} = R_i + R_{av}, \tag{3}$$

where $R_{Ti} = R_{T1}R_{T2}/(R_{T1} + R_{T2})$, R_i is the thermal resistance for the ac component of the pulsed power, R_{av} is the thermal resistance for the dc component of the pulsed power, R_{T1} is the thermal resistance for the time-dependent component of the pulsed power $P_\sim$ generated from the side of region I, and R_{T2} is the thermal resistance for $P_\sim$ generated from the side of regions II and III.

Let us consider procedures for calculating the components of Eq. (3). When the condition $t_i \le (2-3)\tau_{r1}$ is satisfied for the section $X = 0$ in which the diode heating temperature is at a maximum, R_{T1} is written as [12]

$$R_{T1} = \frac{2}{\lambda_1}\sqrt{\frac{\chi_1 t_i}{\pi}}/S, \tag{4}$$

where S is the diode mesa structure area, λ_1 is the thermal conductivity of region I material (silicon), and χ_1 is the silicon thermal diffusivity.

For the IMPATT diodes considered in this study, the doping level of the active layer is quite high. The concentrations of acceptors in the p-type layer and donors in the n-type layer are almost identical, $\sim 3.0 \times 10^{16}$ cm^{-3}. Therefore, we can assume that the thermal conductivity λ and thermal diffusivity χ for the active layer and n^+- and p^+-type layers are approximately identical. According to [13], let us suppose that $\lambda_1 = \lambda_2 \approx 0.8$ W/cm K, $\chi_1 \approx \chi_2 \approx 0.5$ cm^2/s.

The quantity R_{T2} is controlled by nonstationary thermal processes in regions II (R'_{T2}) and III (R'_{T3}) and can be written as

$$R_{T2} = R'_{T2} + R'_{T3}, \tag{5}$$

where R'_{T2} and R'_{T3} are defined for variable power fluxes.

The value of R'_{T2} can be found for steady-state conditions at a continuous power flux as

$$R'_{T2} = \frac{l_2}{\lambda_2 S}, \tag{6}$$

where χ_2 is the thermal conductivity of the region II material (silicon).

We note that R'_{T2} calculation by (6) yields a somewhat overestimated thermal resistance in comparison with the thermal resistance of region II under nonstationary thermal conditions. However, at $t_i \gg \tau_{r2}$, where $\tau_{r2} = l_2^2/4\chi_2$ is the thermal relaxation time of layer II of thickness l_2, the use of (6) for calculating R'_{T2} can be considered acceptable. For the pulsed IMPATT diode designs considered in this study, $l_2 \le 1.5$ μm. Thus, $\tau_{r2} \le 10$ ns, which is significantly shorter than typical durations of operating current pulses $t_i \approx 50$–300 ns of pulsed mm-range IMPATT diodes.

According to [11], R'_{T3} is given by

$$R'_{T3} = \frac{(\chi_3 t_i)^{1/2}}{S\lambda_3} \times \left[\frac{2}{\sqrt{\pi}} - 2\left\{\frac{1}{\sqrt{\pi}}e^{-R^2/4\chi_3 t_i} - \frac{r}{2(\chi_3 t_i)^{1/2}}\operatorname{erfc}\frac{r}{2(\chi_3 t_i)^{1/2}}\right\}\right], \tag{7}$$

where r is the radius of the diode mesa structure and χ_3 is the thermal diffusivity of the heat sink material (copper). It is clear that, at $t_i < \tau_{r3}$, where $\tau_{r3} = r^2/4\chi_3$ is the time of thermal relaxation into the heat sink; R_T components in Eq. (3) can be calculated within one-dimensional consideration of thermal processes in the diode.

In this case, Eq. (7) becomes significantly simpler,

$$R'_{T3} = \frac{2}{\lambda_3}\sqrt{\frac{\chi_3 t}{\pi}}/S, \tag{8}$$

where $t = t_i - \tau_{r2}$.

For IMPATT diodes, according to [1], the equation of the diode thermal resistance under steady-state conditions is written as

$$R_{TP} = \left(\frac{l_2}{\lambda_2} + \frac{r}{\lambda_3}\right)/S. \tag{9}$$

Thus, at large Q, when $R_{av} = R_{TP}/Q \ll R_{Ti}$, and when the condition $t_i < \tau_{r3}$ is satisfied, it is convenient to use the thermal resistivity $\rho_T = R_T S$ in calculations.

Let us consider limitations of the adopted model at decreasing duty ratio Q and unchanged pulse duration t_i. It is clear that heat from region I has no time to flow to heat sink III as $t_p - t_i$ decreases. Since $\tau_{r1} \gg \tau_{r2}$ for IMPATT diodes under consideration, we can assume that calculations by formula (3) are acceptable at $(t_p - t_i) \ge 3\tau_{r1}$ or at $Q \ge 3\tau_{r1}/t_i + 1$.

4. RESULTS OF ESTIMATION OF THE THERMAL RESISTIVITY AND EXCESS TEMPERATURE OF THE p–n JUNCTION

The thermal resistivity ρ_T was estimated for the pulsed IMPATT diode on the copper heat sink (the copper thermal conductivity is $\lambda_3 = 3.9$ W/(cm K)), a mesa structure diameter of 240 μm, and an n^+-type substrate thickness of 10 μm. For such diodes, $\tau_{r1} \approx 500$ ns and $\tau_{r2} \le 10$ ns. Therefore, according to the conditions $t_i \le (2$–$3)\tau_{r1}$ and $t_i \gg \tau_{r2}$, Eq. (3) is valid for 50 ns $\le t_i \le$ 500 ns at the duty ratio $Q \ge 30$.

The dependences $\rho_T = f(t_i)$ calculated by formula (3) are shown in Fig. 3. For comparison, there we also show the calculated excess temperatures ΔT of the p–n junction over the ambient temperature at supply currents of 11.3, 15, and 18 A. We can see that the p–n junction overheating at an operating current pulse duration of 250 ns and an amplitude of 11.3–15 A amounts to 270–430°C. Since the diode should also reliably operate as the ambient temperature increases (60°C), the total temperature at the p–n junction under such operating conditions can reach 310–490°C.

For silicon pulsed IMPATT diodes, a temperature limit no higher than 250°C at a generator temperature of 50°C is usually recommended for the p–n junction

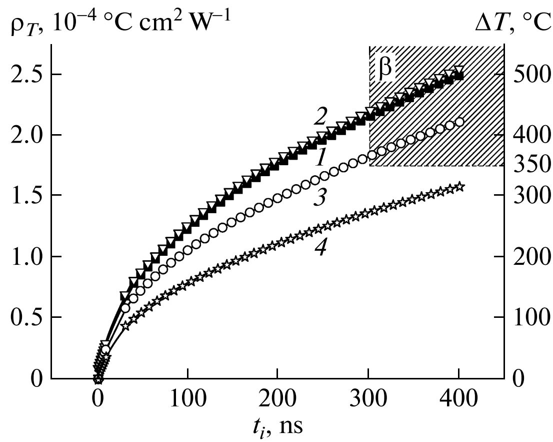


Fig. 3. Dependences of (*1*) the calculated thermal resistivity ρ_T of the IMPATT diode and the excess temperature ΔT at the *p–n* junction over the ambient medium temperature on the pulse duration at diode operating current pulse amplitudes of (*2*) 18, (*3*) 15, and (*4*) 11.3 A. The mesa structure diameter is 240 μm; β is the diode degradation region.

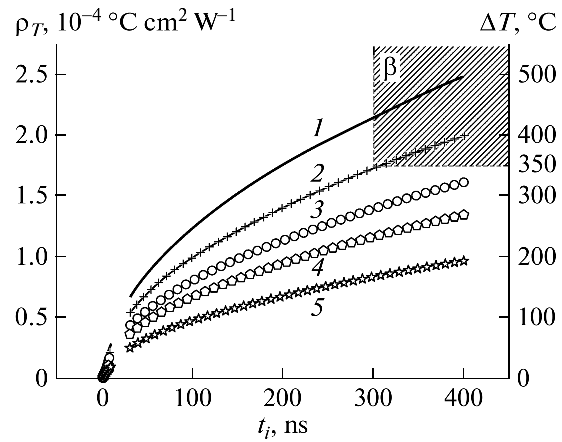


Fig. 4. Dependences of (1) the calculated thermal resistivity ρ_T of the IMPATT diode and the excess temperature ΔT at the *p–n* junction over the ambient medium temperature on the pulse duration at diode operating current pulse amplitudes of (*2*) 22, (*3*) 18, (*4*) 15, and (*5*) 11.3 A. The mesa structure diameter is 285 μm; β is the diode degradation region.

[14]. The temperature limit is determined with the purpose of excluding catastrophic degradation of the mesa structure due to thermal diffusion and electrodiffusion at the silicon–contact-forming layer interface.

If comparatively short diode lifetimes (up to 500 h) are sufficient, a higher overheating temperature of the *p–n* junction of the mesa structure is acceptable. However, the temperature limit in this case can only be restricted to interfacial interactions at the silicon–contact layer interface. For example, in the case of Au penetration through diffusion barriers (buffer layers) to the contact-forming metal–Si interface, an AuSi eutectic can be formed (the eutectic temperature is ~370°C [15]). The thermal breakdown temperature of the silicon mesa structure (360–400°C) can also be a limiting factor. In view of this circumstance, the conditional boundary of an unacceptable excess temperature in the *p–n* junction region can be determined as ~350°C.

The limitations on the maximum acceptable temperature entail the requirement of acceptable operating current amplitudes and pulse durations for given sizes of the mesa structure of the silicon diode. It follows from Fig. 3 that it is not recommended to use such diodes at operating current amplitudes above 15 A and microwave pulse lengths larger than 300 ns. As the mesa structure diameter increases to 285 μm, the acceptable amplitudes of the operating current pulse at a given pulse duration (300 ns) can be increased to 22 A (Fig. 4).

Experimental sets of two-drift silicon IMPATT diodes with mesa structure diameters of 240 and 285 μm were fabricated and studied. The IMPATT diodes with a mesa structure diameter of 240 μm, being incorporated in microwave generators, provided a pulsed microwave power of ≥20 W at a frequency of 33.75 GHz with a minimum time to failure no less than 1000 h at operating current pulse amplitudes of 11–15 A and durations of 300 ns under normal climatic conditions. At the mesa structure diameter of 285 μm and an operating current pulse duration of 300 ns, operating current pulse amplitudes can be in the range of 15–22 A and can provide an output pulsed microwave power of 30–35 W in a frequency range of 32.5–34.5 GHz, which exceeds the level achieved by leading foreign producers [14, 16].

5. INTERPHASE INTERACTIONS IN CONTACT METAL LAYERS CAUSED BY EXCESS TEMPERATURE

To study physicochemical processes in contact metal layers, test structures were subjected to 60-s RTA at 350(450)°C and 10-min TA at the same temperatures in vacuum. It was found that RTA had almost no effect on the component concentration profiles in metallization layers. However, 10-min TAs at 350°C caused weak restructurization in metal layers and 10-min TAs at 450°C caused drastic changes.

Figures 5a–5c show the component concentration profiles in the initial Au–Pt–Ti–Pd–Si test structure and after TA at 350(450)°C in vacuum. We can see that the multilayer structure in the contact coating of the initial sample is retained after 10-min TA at 350°C. However, the Si depth profile is nonmonotonic in both the initial sample and the sample after 10-min TA at 350°C, which can indicate possible phase formation of silicon with palladium even during Pd sputtering [17, 18]. In this case, maximum oxygen and carbon contents are localized in the titanium film and certain

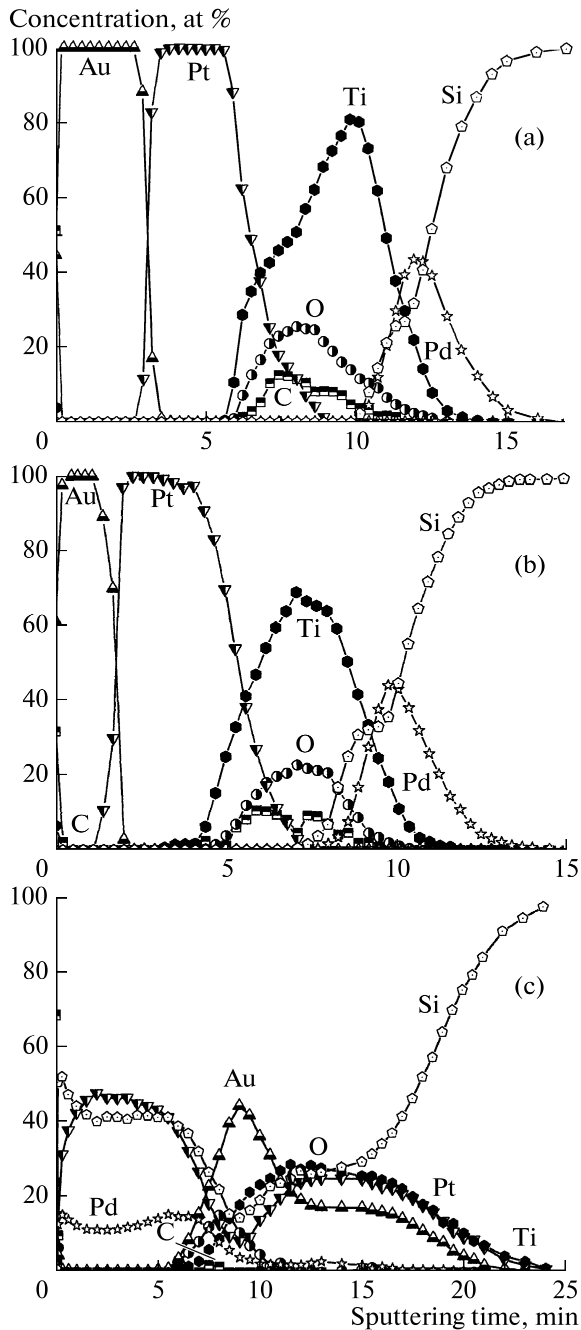


Fig. 5. Component concentration profiles in the Au–Pt–Ti–Pd–Si contact coating in (a) the initial sample and after 10-min TA at (b) 350 and (c) 450°C.

amounts of them are observed in intermediate layers at the Pt–Ti and Pd–Ti interfaces. TA also had no effect on the state of the upper metallization (Au) layer, which was confirmed by the absence of morphological changes on the Au film surface (Fig. 6), although Pt has diffused approximately to half the thickness of the gold film.

The phase composition of the Au–Pt–Ti–Pd–Si contact coating was studied (ex situ) by X-ray diffraction using a Philips X'Pert-MPD X-ray diffractometer (CuK_α, wavelength $\lambda = 0.15418$ nm) in Bragg–Brentano geometry.

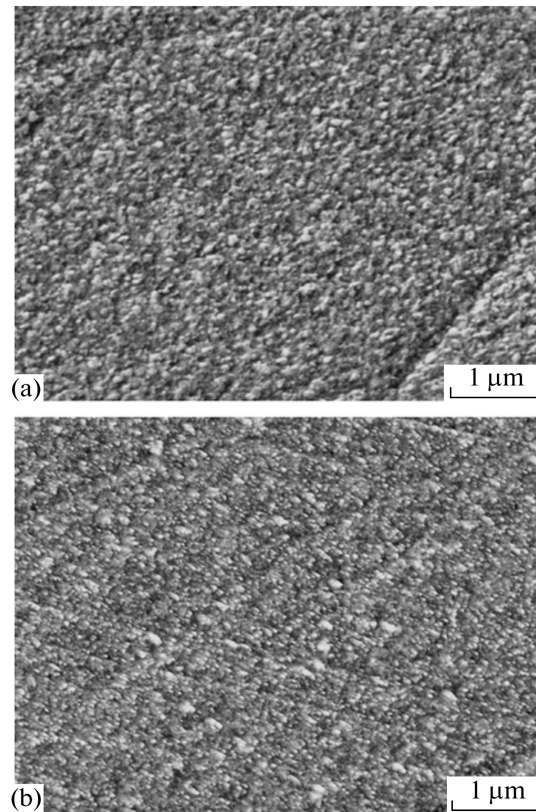


Fig. 6. Surface morphology of the Au film of (a) the initial sample and (b) after 10-min TA at 350°C.

The XRD spectra of the initial Au–Pt–Ti–Pd–Si contact (Fig. 7) contain reflections from the Si (111) substrate at 28.493°, from Pd_2Si, and a set of reflections from Au, Pt, Ti, and Pd metal layers, which indicates their polycrystalline structure. The Pd_2Si phase was probably formed due to the Pd–Si interaction during sputtering onto the substrate heated to 300°C. The presence of polycrystalline Pd points to incomplete Pd_2Si phase formation in the initial sample. The XRD spectrum of the sample annealed at 350°C for 10 min (Fig. 7), in comparison with the spectrum of the initial sample, contained a reflection corresponding to the Pd_3Ti phase.

The 10-min thermal treatment at 450°C distorts the layered structure of the contact coating and causes the formation of an extended mixing region; Si, Pt, and Pd emergence through the Au film to the outer metallization surface; Pt, Ti, and Au penetration into Si; a significant decrease in the carbon content within the mixing region; oxygen displacement to the outer surface; and a significant Au displacement to the mixing region depth (Fig. 5c). The shape of the depth profiles of metal components and silicon and the presence of characteristic flats in these distributions are indica-

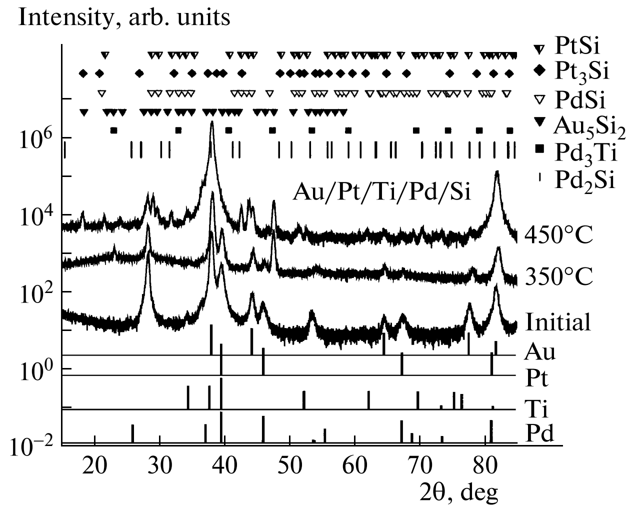
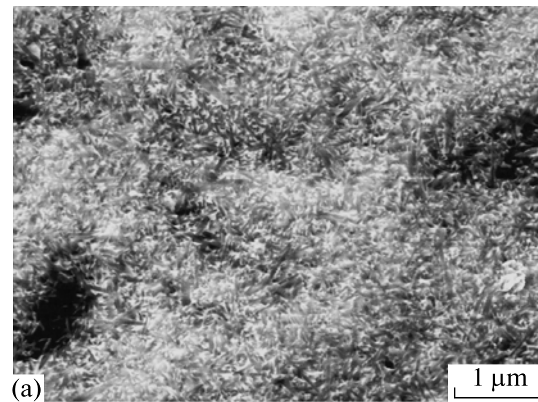
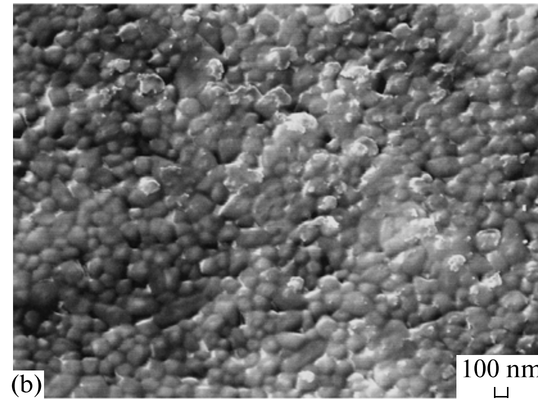


Fig. 7. X-ray diffraction patterns of the initial Au–Pt–Ti–Pd–Si structure, after 10-min TA at 350°C, and after 10-min TA at 450°C.

tive of the possibility of the formation of some phases, including silicide ones, which correlates with the XFA data. X-ray diffraction patterns of this sample (Fig. 7, curve *3*) showed the presence of PtSi, PdSi, Pt_3Si, and Au_5Si_2 phases. Furthermore, two more pronounced maxima at 39 and 82° are observed near reflections of bulk cubic Au, which is indicative of the formation of a solid solution based on Au, which probably includes Au, Pt, Ti, Pd, and Si. An analysis of the XRD spectrum of this sample suggests that complete interdiffusion of components along grain boundaries of polycrystalline films with the formation of a solid solution most likely occurs during 10-min TA at 450°C. Another factor enhancing mass transfer during TA is the presence of pores resulting from TP-stimulated relaxation of internal mechanical stresses in contact metallization layers. Figure 8 shows the surface morphology fragments of the Au–Pt–Ti–Pd–Si test structure annealed at 450°C for 10 min. We can see that the Au film surface is covered by pores (Figs. 8a, 8b), the sizes of which are within 0.1–1 μm. Some film surface areas of such test structures contain defects the nature of which is probably related to relaxation of internal mechanical stresses in the region of stress concentrators (Fig. 8c), the role of which can be played by phase inclusions.

Thus, the results of structural studies and Auger electron spectrometry show that 10-min TA at 350(450)°C, even without electrical load simulation, results in phase formation in the Au–Pt–Ti–Pd–Si contact coating at 350°C and total deterioration of the layered structure after TA at 450°C, which confirms the above evaluations of the role of the excess temperature at the *p*–*n* junction over the ambient medium temperature in IMPATT diode degradation.





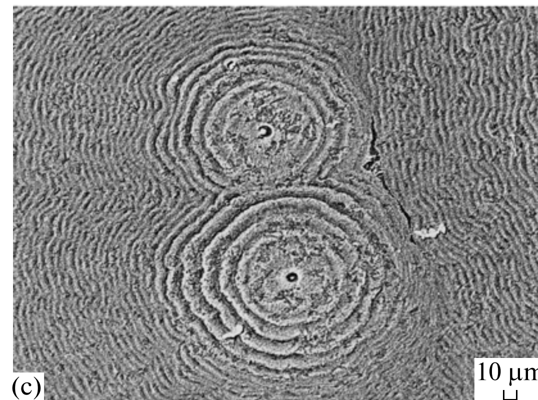


Fig. 8. Surface morphology of the Au film after 10-min TA at 450°C: (a, b) surface fragments with different magnifications; (c) surface fragment with relaxation of internal mechanical stresses in the region of stress concentrators.

6. CONCLUSIONS

Thus, for high-power pulsed silicon two-drift IMPATT diodes of the 8-mm wavelength region, the limiting temperature of the *p*–*n* junction was determined as 350°C, above which IMPATT diodes actively degrade. Based on this temperature, a pulsed mode of IMPATT diodes providing their long-term operation was proposed.

To increase the lifetime of high-power pulsed IMPATT diodes, it is necessary to search for a contact metallization type with diffusion barriers not interacting with Si and adjacent metal layers to temperatures above 350°C.

REFERENCES

1. A. S. Tager and V. M. Val'd-Perlov, *Avalanche-Transit-Time Diodes and Their Applications in UHF Electronics* (Sov. Radio, Moscow, 1968), ch. 9, p. 374; ch. 7, p. 335 [in Russian].
2. A. K. Shukhostanov, *Avalanche-Transit-Time Diodes. Physics, Technology, Application* (Radio i svyaz', Moscow, 1997), ch. 7, p. 157 [in Russian].
3. L. V. Kasatkin and V. P. Rukin, Izv. Vyssh. Uchebn. Zaved., Ser. Radioelektron. **48** (6), 3 (2005).
4. L. V. Kasatkin and V. E. Chaika, *Semiconductor Devices of Millimeter Range* (Sevastopol', Veber, 2006) ch. 1, p. 32; ch. 2, p. 132 [in Russian].
5. G. Haddad and R. Trew, IEEE Trans. MTT-S **50**, 760 (2002).
6. H. Eisele and G. Haddad, IEEE Trans. MTT **46**, 739 (1998).
7. V. F. Oleinik, V. L. Bulgach, V. V. Valyaev, A. V. Zorenko, D. V. Mironov, and V. E. Chaika, *Electron Devices of Millimeter and Submillimeter Ranges on the Basis of Nanotechnology* (GNIKT, Kiev, 2004) [in Russian].
8. V. V. Basanets, N. S. Boltovets, A. V. Zorenko, A. V. Gutsul, N. V. Kolesnik, and S. I. Gerashchenko, Tekhn. Pribory SVCh, No. **1**, 27 (2009).
9. N. S. Davydova and Yu. Z. Danyushevskii, *Microwave Diode Oscillators and Amplifiers* (Radio i svyaz', Moscow, 1986), ch. 5, p. 143 [in Russian].
10. A. S. Tager, Elektron. Tekhn., Ser. Elektron. SVCh **5**, 3 (1981).
11. G. Gibbons, Solid State Electron. **13**, 799 (1970).
12. G. Carslaw and D. Jaeger, *Conduction of Heat in Solids* (Oxford Univ., Oxford, 1986; Inostr. Liter., Moscow, 1964).
13. *Physical Quantities. A Manual*, Ed. by I. S. Grigoriev and E. Z. Meilikhov (Energoatomizdat, Moscow, 1991), p. 341 [in Russian].
14. http://www.quinstar.com
15. M. Hansen and K. Anderko, *Structure of Binary Alloys* (McGraw-Hill, New York, 1958; Metallurgizdat, Moscow, 1962), vol. 1, p. 253.
16. http://www.microsemi.com
17. S. P. Murarka, *Silicides for VLSI Application* (Academic, New York, London, 1983; Mir, Moscow, 1989), ch. 2, p. 59.
18. A. E. Gershinskii, A. V. Rzhanov, and E. I. Cherepov, Mikroelektronika **11** (2), 86 (1982).

Translated by A. Kazantsev