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Thin-film solar converters based on the *p*-$Cu_{1.8}S$/*n*-CdTe surface-barrier structure

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Abstract. A surface-barrier structure with the transparent *p*-$Cu_{1.8}S$ component was used to make thin-film polycrystalline *n*-CdTe-based solar converters. Cadmium telluride was grown on CdSe substrates using the quasi-closed volume technique through a graded-gap $CdSe_xTe_{1-x}$ interlayer. A multilayer *p*-$Cu_{1.8}S$/*n*-CdTe/*n*-CdSe/Mo structure was prepared. It makes it possible to increase the degree of structural perfection of thin photosensitive *n*-CdTe layers without application of additional high-temperature treatments, as well as to obtain an ohmic back contact without some additional doping of CdTe. The quantum efficiency spectra and critical parameters of solar converters have been presented. The prospects for application of polycrystalline *n*-CdTe in solar power engineering have been discussed.

Keywords: solar converter, cadmium telluride, copper chalcogenide, graded-gap layer, surface-barrier structure.

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1. Introduction

The developments of thin-film solar converters (SC) have reached the stage of mass manufacturing application. The most competitive SC are those made of amorphous silicon (a-Si:H), cadmium sulfide-telluride CdS-CdTe and copper-indium (or copper-gallium) diselenide CdS-Cu(In, Ga)Se_2. The efficiency η of laboratory patterns of the above SC reaches 10, 16 and 18%, respectively.

The advantages of CdTe-based SC [1-7] are their effectiveness, possibility of making SC on flexible substrates (high specific power) and high radiation resistance. A thin CdS layer in an efficient *n*-CdS/*p*-CdTe structure is non-photoactive and serves as a wide-gap window. The polycrystalline *p*-CdTe acts as a photosensitive SC component.

The results obtained using the single crystal *n*-CdTe are less impressive (efficiency up to 9% only [8, 9]). Since the optimal *p*-type wide-gap window for *n*-CdTe is not known, only the possibility of Schottky barrier diode application was discussed in literature. The small achievements are related to bad parameters of the corresponding barrier structures. In addition (when dealing with polycrystalline layers), a drawback of metal-semiconductor contacts is complexity of obtaining a continuous thin metal film on a relief surface of polycrystalline semiconductor.

New prospects for the development of barrier structures are related to the existence of an effective match with *n*-type II–VI semiconductors, namely, digenite *p*-$Cu_{1.8}S$ (stable strongly degenerate modification of copper chalcogenide) [10-13]. The advantages of using *p*-$Cu_{1.8}S$ instead of metal in surface-barrier photoconverters are related with the rather high work function (~5.5 eV) and possibility of growing nanometer (~10 nm) $Cu_{1.8}S$ film on the surface of polycrystalline II–VI layers.

In this work, we report on fabrication of $Cu_{1.8}S$/CdTe SC (based on polycrystalline *n*-CdTe) and studying its main properties.

2. Fabrication of polycrystalline solar converters

The main requirements for polycrystalline CdTe layers serving as the photosensitive part of SC are as follows:

1. The layers must be textured, with crystallites of optimal sizes, thus making it possible to minimize current losses at intercrystallite interlayers of the polycrystalline layer. To improve the structural properties of *p*-CdTe, manufacturing technology for CdS-CdTe SC must include a high-temperature “chloride” treatment. It results in crystallite growth as well as promotes diffusion of Te and Cu acceptor impurities into the CdTe layer [1, 4].
2. The layers must have a reliable ohmic back contact. The molybdenum back electrode is coated with Te and Cu films before CdTe layer deposition on it to improve ohmic contact to polycrystalline *p*-CdTe.
3. The layers must be sufficiently low-resistant. To meet this requirement for polycrystalline CdTe layers, doping with the corresponding impurity has to be made. In this case, one has to take into account difficult-to-control predominant diffusion of foreign impurity over the intercrystallite interlayers. This process impairs reproducibility of manufacturing technology for solar cells and may lead to degradation of their properties. To illustrate, one of the main mechanisms of degradation of *p*-CdTe based SC is copper diffusion into the region of CdS-CdTe heteroboundary from the back electrode [4]. Indium diffusion from CdS into the *p*-CdTe layer results in reduction of the solar cell efficiency [1].

In our work, we study the possibility to solve the above-mentioned problems for *n*-CdTe by its epitaxial growing on orienting polycrystalline *n*-CdSe substrates. A graded-gap $CdSe_xTe_{1-x}$ interlayer was grown to exclude the mechanism of formation of structural defects related to a mismatch between the CdSe and CdTe lattice parameters.

Using the quasi-closed volume technique, the graded-gap CdSe layer and *n*-CdTe were sequentially deposited, in the common technological cycle, onto the Mo-metallized glass-ceramic substrates. Molybdenum serves as the reliable ohmic electrode to the CdSe layer. So, CdTe growing on the Mo-CdSe substrate through a graded-gap interlayer solves the problem of obtaining ohmic contact to photosensitive polycrystalline *n*-CdTe layer without additional doping. Growing *n*-CdTe on the orienting *n*-CdSe substrates through a graded-gap interlayer solves also the problem of obtaining textured (with optimal crystallite sizes) photosensitive *n*-CdTe layers without additional high-temperature treatment of the multilayer SC structure.

Fig. 1 presents the results of investigation of specimen surfaces performed with a scanning probe microscope NanoScope IIIa Dimension 3000^{TM} (Digital Instruments, USA) using atomic force microscopy (AFM) in the periodic contact mode. The silicon probes with nominal tip radius of 10 nm were used in measurements.

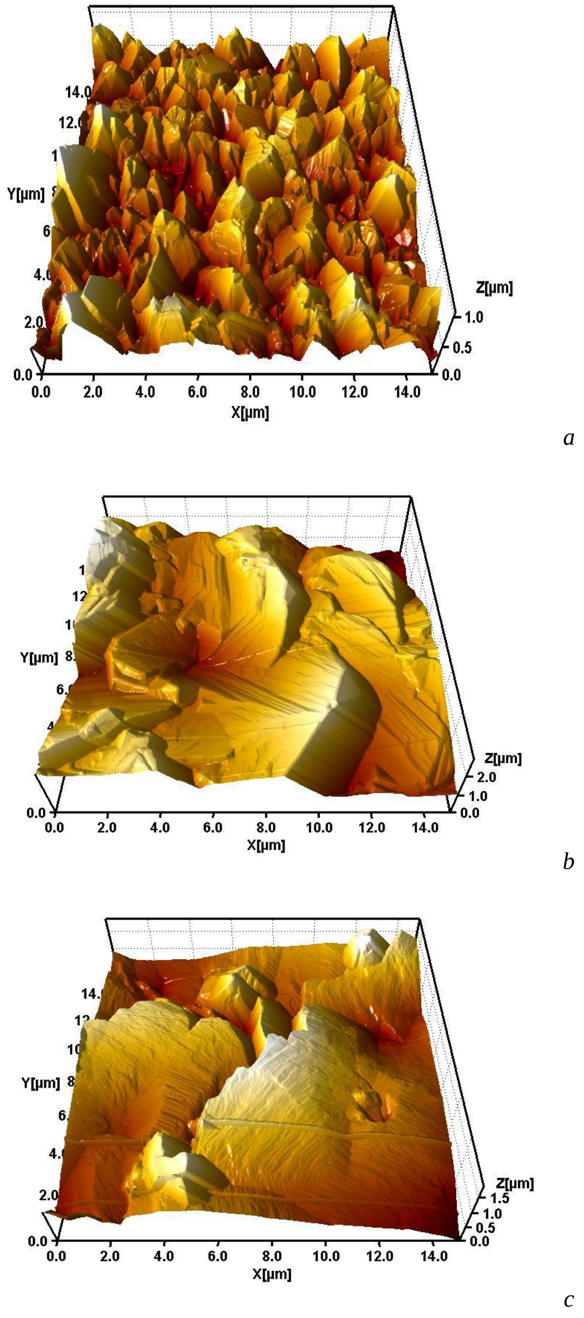

Fig. 1. AFM patterns of surface fragments of CdTe specimens grown on different substrates: a) Mo-metallized glass-ceramics, b) Mo/CdSe, c) Mo/$CdSe_xTe_{1-x}$/CdSe.

We studied the surfaces of CdTe specimens grown on different substrates. In the case of Mo-metallized glass-ceramic substrate for CdTe (Fig. 1a), the characteristic crystallite size is 1.4 μm (standard deviation of 0.425 μm). The large to little ratio is sufficiently high: 2.455/0.698. For the Mo/CdSe/CdTe structure (Fig. 1b), the average grain size is essentially larger: 6.7 μm. The large to little ratio decreased to 8.06/5.31 μm. For a CdTe specimen on the Mo/CdSe substrate with a graded-gap $CdSe_xTe_{1-x}$ interlayer of about 100 nm (Fig. 1c), the surface character changed. The crystallites demonstrate a trend to formation of a plateau of about 13 μm with growth terraces.

The above results testify that it is possible to obtain a sufficiently perfect thin CdTe film of an optimal thickness (1…2 μm) with large crystallites without additional high-temperature treatment of the structure.

To make SC, a barrier-forming layer of *p*-type copper sulfide (its stable modification $Cu_{1.8}S$) was deposited on CdTe surface using the vacuum sputtering. The SC structure has the attributes of the surface-barrier one: electric field is practically completely concentrated in *n*-CdTe owing to sharp doping asymmetry in the contacting materials (the hole concentration in $Cu_{1.8}S$ $p = 5\cdot10^{21}\,\mathrm{cm}^{-3}$). The total structure thickness is 4…5 μm, while that of the graded-gap layer is 100…200 nm. The SC series resistance is determined by the resistances of the CdSe and CdTe layers, which thicknesses are 3…4 and 1.5 μm, respectively. The structure is illuminated from the side of the transparent component of copper sulfide $Cu_{1.8}S$, thickness of which was 20…30 nm.

It is possible to obtain sufficiently low-resistant polycrystalline CdSe layers without additional doping with a foreign impurity. It is known [14] that one can vary the concentration of free charge carriers within wide limits in the specimens obtained by regulating the concentration of intrinsic defects of crystal lattice when changing the manufacturing conditions for CdSe crystals (as opposed to CdTe). The concentration of majority charge carriers in polycrystalline CdSe crystals grown without additional doping with a foreign impurity was $(1\ldots2)\cdot10^{16}\,\mathrm{cm}^{-3}$. It was sufficient for keeping the series resistance of the structure within admissible limits.

The situation with CdTe is more complicated. One cannot obtain CdTe layers with the electron concentration $n > 10^{13}\,\mathrm{cm}^{-3}$ by using the quasi-close volume technique. The effect of intergrowth of donor-type point defects from the CdSe substrate to *n*-CdTe through a developing graded-gap interlayer (which is characteristic of ZnS and ZnSe [10, 12]) was not observed in the multilayer structures under investigation. The electron concentration did not exceed $10^{14}\,\mathrm{cm}^{-3}$, which is obviously not enough for efficient operation of SC.

So, additional doping of SC with a foreign impurity is required to ensure the use of *n*-CdTe layers. In this work, CdTe was doped with indium in the course of growing to determine the potential of *n*-CdTe-based SC.

3. Experimental results

Fig. 2 presents the energy band diagram of the system *p*-$Cu_{1.8}S$/*n*-CdTe/*n*-CdSe/Mo SC. A reliable ohmic contact of the CdSe layer with Mo-metallized glass-ceramic substrate (the latter is not shown in Fig. 2) ensures the ohmic back contact of the multilayer heterostructure. The diagram corresponds to the case of relatively high-resistant CdTe (charge carrier concentration $n = 10^{13}\,\mathrm{cm}^{-3}$). The diffusion potential $U_d \approx 0.87$ eV. It is evident that increase of the concentration of majority charge carriers leads to increase of U_d and, consequently, improves the SC diode characteristics.

Forward recombination-tunnel currents (that are typical for the *p*-$Cu_{1.8}S$/*n*-II–VI junctions [11-13]) are predominant in the structures under investigation. The observed minimal densities of dark diode currents are $(2\ldots3)\cdot10^{-8}\,\mathrm{A/cm}^2$.

Fig. 3 presents dependences of the quantum efficiency *H* and charge carrier collection coefficient *Q* on the wavelength of radiation incident on *p*-$Cu_{1.8}S$/*n*-CdTe SC. To analyze photocarrier losses, let us present the photocurrent I_{ph} in the structures under investigation as

$$I_{ph} = eTQ = eTQ_sQ_L.$$

Here, *T* is the intensity of light that is part of the photosensitive component (in the limiting case this is transmission of the $Cu_{1.8}S$ layer); the coefficients Q_s and Q_L characterize photocarrier losses on the illuminated surface at the *p*-$Cu_{1.8}S$/*n*-CdTe junction interface and in the CdTe bulk, respectively.

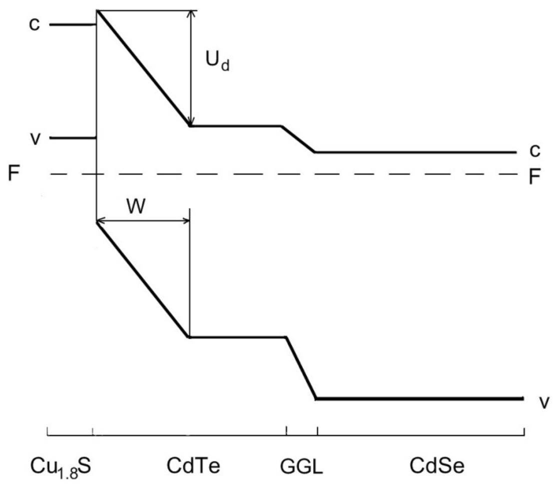

Fig. 2. Energy band diagram of the *p*-$Cu_{1.8}S$/*n*-CdTe/*n*-CdSe/Mo solar converter: F is the Fermi level, *W* – space-charge region width, GGL – graded-gap layer.

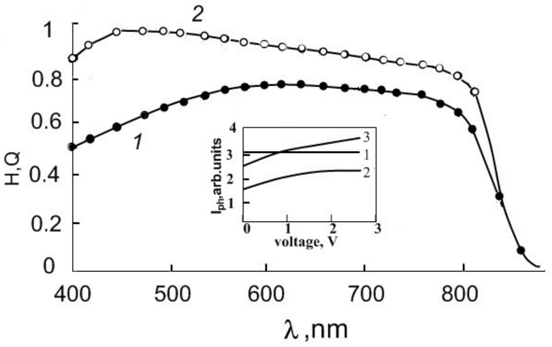

Fig. 3. Spectral dependences of quantum efficiency *H* and charge carrier collection coefficient *Q* of solar converters.

One can see from Fig. 3 that there is a peak in the curve, and Q values are close to unity. The latter fact is supported by the results of investigations of field dependences (photocurrent vs negative bias voltage). As the voltage U increases, the photoactive region becomes broader, the width of space-charge region W grows and the sweeping field at the illuminated SC surface becomes stronger. These factors have to promote increase of efficiency in the long-wave and short-wave spectral regions, if $Q < 1$.

Shown in Fig. 3 (inset) are the dependences $I_{ph}(U)$. One can see (inset, curve 1) that, if SC is illuminated with light with the wavelength is $\lambda = 0.45$ µm, then I_{ph} does not depend on U. The most probable reason for the above effect is absence of photocurrent losses in the given spectral region and, consequently, $Q = 1$. At $\lambda = 0.4$ µm, photocurrent flattens out as U increases (inset, curve *2*). In this case, the value of Q is determined as the ratio between the short-circuit current ($U = 0$) and the photocurrent I_{ph} value at saturation; then the quantum efficiency is $Q = 0.87$.

The obtained results testify that photocurrent losses in the long-wave spectral region ($\lambda > 0.45$ µm) is determined only by recombination of charge carriers in the quasi-neutral region of CdTe, and growth of I_{ph} (inset, curve *3*) is because of increase in the space-charge region width W. Then, the photocurrent can be written as

$$I_{ph} = eTQ_L = eT\{1 - [\exp(-\alpha W)]/(1 + \alpha L_p)\},$$

where α is the coefficient of light absorption in CdTe, and L_p is the hole diffusion length. For those SC specimens, in which the above situation is realized, L_p values were determined using the method proposed in [15].

At $\alpha W >> 1$, the photocurrent $I_{ph} = eTQ_L = eT(L_p + W)/(1 + \alpha L_p)$ is a linear function of the space-charge region width W. Extrapolation of the linear dependence $I_{ph}(W)$ from the region of high U values to zero photocurrent determines the diffusion length L_p of minority charge carriers. When determining L_p, the specimens were illuminated with light of the wavelength $\lambda = 0.84$ µm. The dependences $I_{ph}(W)$ are well presented by straight lines. The hole diffusion length L_p lies within 0.6…0.8 µm for different SC specimens under investigation.

The main operating parameters of SC were measured under natural solar illumination. The emittance of incident radiation was measured with a pyranometer M-80M and was 0.74 mW/cm^2. The best parameters were those measured for $Cu_{1.8}S$-CdTe SC, in which CdTe was doped with indium. At the above emittance of incident radiation, this SC demonstrated the peak open-circuit emf $U_{oc} = 0.71$ V, fill factor (FF) of load characteristic FF = 0.7, short-circuit current density $I_{sc} = 15.8$ mA/cm^2, efficiency $\eta = 10.7\%$. The SC area (with allowance made for ~10% shadowing with the upper current-collecting electrode) was $s = 0.25$ cm^2.

4. Conclusion

Strongly degenerate digenite $Cu_{1.8}S$ is the optimal *p*-component for fabrication of *p*-$Cu_{1.8}S$-*n*-II–VI surface-barrier structures that can serve as the basis for making efficient photoconverters of UV and visible radiation. Our investigations performed in this work have shown that the above surface-barrier structure is promising for application in solar power engineering. The potentialities for achievement of good parameters in *n*-CdTe-based SC are close to those known for *p*-CdTe-based SC.

We propose the method of growing *n*-CdTe that makes easier a number of technological operations inherent to manufacturing technology for *p*-CdTe. Cadmium telluride is grown on the Mo/CdSe substrates through a graded-gap $CdSe_xTe_{1-x}$ interlayer. The structure of *p*-$Cu_{1.8}S$/*n*-CdTe/*n*-CdSe/Mo SC enables one to increase the degree of structural perfection of *n*-CdTe photosensitive layers without additional high-temperature treatments as well as to obtain back ohmic contacts without additional doping of CdTe. The sufficiently high quantum efficiency obtained for *n*-CdTe is close to the limiting one for the $Cu_{1.8}S$/*n*-CdTe structure. The feasible way for increasing SC efficiency with the above structure is related with improvement of the diode characteristics of the surface-barrier structure and, consequently, increase of U_{oc} and the fill factor of load characteristics FF.

The above improvements require maximal doping of CdTe with a donor impurity. So, a search for a method of doping polycrystalline CdTe layers that could minimize the probability of separating barrier shorting is urgent. It is necessary to increase both reproducibility of manufacturing technology and stability of properties inherent to polycrystalline SC.

References

1. Kasturi Lal Chopra, Suhit Ranjan Das, *Thin Film Solar Cells*. Plenum Press, New York, London (1983).

2. B.T. Boyko, V.B. Yurchenko, G.I. Kopach, A.S. Opanasjuk, G.S. Hripunov, V.A. Polotski, Photoelectric properties of CdTe-based film heterojunctions with graded-gap interlayers // *Bulg. J. Phys.* **14**(2), p. 157-162 (1987), in Russian.
3. D. Bonnet, P. Meyers, Cadmium telluride – materials for thin film solar cells // *J. Mater. Res.* **13**(10), p. 2740-2753 (1999).
4. A. Romeo, D.L. Bätzner, H. Zogg, A.N. Tiwari, A comparison of the vacuum evaporated CdTe substrate and superstrate solar cells, in: *Proc. 16th European Photovoltaic Solar Energy Conf. and Exhibition* (*Glasgow, 2000*), p. 843-846.
5. G.S. Khripunov, B.T. Boyko, Flexible ITO/CdS/CdTe/Cu/Au solar cells with high specific power // *Fizicheskaya Inzheneriya Poverkhnosti*, **2**(1-2), p. 69-73 (2004), in Russian.
6. G.S. Khrypunov, E.P. Chernykh, N.A. Kovtun, E.K. Belonogov, Flexible solar cells based on cadmium sulfide and telluride // *Fizika Tekhnika Poluprovodnikov*, **43**(8), p. 1084-1089 (2009), in Russian [*Semiconductors,* **43**(8), p. 1046-1051 (2009)].
7. J.G. Werthen, J.P. Haring, A.L. Fahrenbruch, R.H. Bube, Surface effects on metal-CdTe junctions and CdTe heterojunctions // *J. Phys. D: Appl. Phys.* **16**(12), p. 2391-2404 (1983).
8. J.P. Ponpon, P. Siffert, Barrier heights on cadmium telluride Schottky solar cells // *Rev. Phys. Appl.* **12**(2), p. 427-430 (1977).
9. G. Fulop, M. Doty, P. Meyers, J. Betz, C.H. Liu, High-efficiency electrodeposited cadmium telluride solar cells // *Appl. Phys. Lett.* **40**(4), p. 327-328 (1982).
10. Yu.N. Bobrenko, A.M. Pavelets, S.Yu. Pavelets, V.M. Tkachenko, Short-wavelength photosensitivity of surface-barrier structures with degenerate semiconductor-semiconductor junctions // *Pis'ma v ZhTF*, **20**(12), p. 9-13 (1994) (in Russian); *Tech. Phys. Lett.* **20**, p. 477-480 (1994).
11. Yu.N. Bobrenko, S.Yu. Pavelets, A.M. Pavelets, The efficient photoelectric converters of UV radiation with ZnS-based graded-gap layers // *Fizika Tekhnika Poluprovodnikov,* **43**(8), p. 830-835 (2009), in Russian [*Semiconductors*, **43**, p. 801-805 (2009)].
12. Yu.N. Bobrenko, S.Yu. Pavelets, A.M. Pavelets, M.P. Kiselyuk, N.V. Yaroshenko, Efficient photoelectric converters of ultraviolet radiation based on ZnS and CdS with low-resistivity surface layers // *Fizika Tekhnika Poluprovodnikov*, **44**(8), p. 1114-1117 (2010) (in Russian) [*Semiconductors,* **44**(8), p. 1080-1083 (2010)].
13. Yu.N. Bobrenko, S.Yu. Pavelets, A.M. Pavelets, N.V. Yaroshenko, Photoelectric converters with graded-gap layers based on ZnSe // *Semiconductors*, **47**(10), p. 1372-1375 (2013).
14. *Physics of II–VI Compounds*, ed. by A.N. Georgobiani and M.K. Sheinkman. Nauka, Moscow, 1986 (in Russian).
15. W.W. Gartner, Depletion-layer photoeffects in semiconductors // *Phys. Rev.* **116**(1), p. 84-87 (1959).